

(19)



Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 1 134 811 A1

(12)

EUROPEAN PATENT APPLICATION

published in accordance with Art. 158(3) EPC

(43) Date of publication:
19.09.2001 Bulletin 2001/38

(51) Int Cl.7: **H01L 29/786**, H01L 29/73,
H01L 29/80

(21) Application number: **99972374.5**

(86) International application number:
PCT/JP99/06300

(22) Date of filing: **11.11.1999**

(87) International publication number:
WO 00/30183 (25.05.2000 Gazette 2000/21)

(84) Designated Contracting States:
AT BE CH DE FR GB LI NL

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(30) Priority: **17.11.1998 JP 32688998**

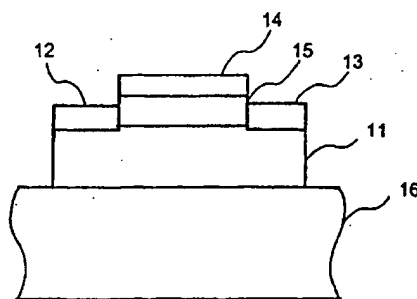
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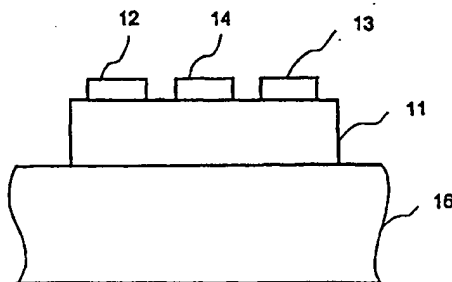
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(54) TRANSISTOR AND SEMICONDUCTOR DEVICE

(57) A transistor is provided, which is entirely and partially transparent by the use of a transparent channel layer made of zinc oxide or the like. A channel layer 11 formed of a transparent semiconductor such as zinc oxide ZnO. A transparent electrode is used for all of a source 12, a drain 13 and a gate 14, or a part of them. As the transparent electrode, a transparent conductive material such as conductive ZnO doped with, for example, group III elements is used. As a gate insulating layer 15, a transparent insulative material such as insulative ZnO doped with elements capable of taking a valence of one as a valence number or group V elements is used. If a substrate 16 must be transparent, for example, glass, sapphire, plastic or the like can be used as a transparent material.



(A)



(B)

Fig 1

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Description

Field of the Invention

[0001] The present invention relates to a transistor and a semiconductor device, more particularly to a transparent transistor, a semiconductor device having the transparent transistor stacked thereon, and a semiconductor device to which the transparent transistor is applied for driving a light emission device, for reading/writing data from/to a memory, and for other purposes. It should be noted that in the present invention, a concept of "transparent" includes a concept of "being transparent or offering light transmission property" for the sake of simplifying descriptions.

Descriptions of the Related Arts

[0002] A thin film transistor using amorphous silicon, polycrystalline silicon or the like has been generally used as a transistor for use in driving liquid crystal display devices. Since these materials exhibit photosensitivity for the visible light region, carriers are generated by a beam of light, and resistivity of a thin film constituting the thin film transistor is lowered. For this reason, when the beam of light is radiated thereonto, the transistor may be made to be a turn-on state, in spite of the fact that the transistor must be controlled to be a turn-off state. Accordingly, to keep the transistor at the turn-on state, the lowering of the carrier resistivity of the thin film due to the radiation of the beam of light has been heretofore prevented by the use of a light shielding layer made of a metal film or the like.

Disclosure of the Invention

[0003] Generally, the liquid crystal display device has been widely used for a notebook type personal computer or the like, and an energy-saving measure, a high luminance and a miniaturization have been requested of the liquid crystal display device. To reply to these requests, it is effective to increase a rate of an effective area of a display portion within a unit pixel. However, since a light shielding layer made of a metal thin film or the like in the transistor for driving the liquid crystal display device is formed as described above, a rate of an area of a light transmission portion to that of the light shielding layer (opening ratio) in the pixel reduces. Accordingly, a reduction of a transistor area by improving a performance of the transistor or an improvement of luminance of a backlight are necessary to develop a display device having high luminance. However, the measure to improve the characteristic of the transistor shows a limitation to a yield, leading to an increase in cost. Moreover, the measure to improve the luminance of the backlight increases an amount of energy consumption.

[0004] From the viewpoint of the above described points, the object of the present invention is to provide

a transistor using a transparent channel layer made of zinc oxide or the like, which is transparent partially or entirely, because an orientation control of the zinc oxide and a valence electron control thereof that has been heretofore difficult is now possible. Specifically, the object of the present invention is to provide a transistor which uses a transparent material such as the zinc oxide or the like for a channel layer (conductive layer) so that the channel layer does not have a photosensitivity for the visible light region, and removes a necessity to form a light shielding layer, thus increasing an area rate of a display portion of a liquid crystal display device or the like.

[0005] Furthermore, the object of the present invention is to use a transparent transistor for various kinds of applications in an optical device field for use in driving a light emission device such as a plane light emission laser and an electroluminescence device and for use in a memory. Still furthermore, the object of the present invention is to provide a semiconductor device used as a transparent electronic device for various kinds of wide applications in addition to a driving circuit requiring no light shielding layer.

[0006] According to first solving means of the present invention, a transistor is provided, which comprises:

a transparent channel layer using any one of zinc oxide ZnO, zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$ and cadmium oxide CdO; and

a source, a drain and a gate in which a transparent conductive material such as conductive ZnO doped or undoped with any one of group III elements, group VII elements, group I elements and group V elements, a transparent conductive material such as In_2O_3 , SnO_2 and $(In-Sn)O_x$, or an untransparent electrode material are used partially or entirely.

[0007] According to second solving means of the present invention, a transistor is provided, which comprises:

an emitter and a collector, or a base which are made of a transparent n-type semiconductor such as ZnO doped with group III elements or group VII elements;

a base, or an emitter and a collector which are made of a transparent p-type semiconductor such as ZnO doped with group I element or group V elements; and

a base electrode, an emitter electrode and a collector electrode respectively formed on the base, the emitter and the collector, in which a transparent conductive material such as conductive ZnO doped or undoped with any one of group III elements, group VII elements, group I elements and group V elements, a transparent conductive material such

as InO_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$, or an untransparent electrode material are used partially or entirely.

[0008] Still another object of the present invention is to provide a semiconductor device in which a transparent transistor is stacked, and a semiconductor device applied to a light emission device, a memory or the like.

Brief Descriptions of the Drawings

[0009] Figs. 1(A) and 1(B) are section views of a first embodiment of a transistor according to the present invention.

[0010] Figs. 2(A) and 2(B) are section views of second and third embodiments of a transistor according to the present invention.

[0011] Fig. 3 is a section view of a fourth embodiment of a transistor according to the present invention.

[0012] Fig. 4 is a section view of a fifth embodiment of a transistor according to the present invention.

[0013] Fig. 5 is a section view of a stacked type semiconductor device.

[0014] Figs. 6(A) and 6(B) are a section view and a circuit diagram of a semiconductor device to which a FET according to the present invention is applied for driving a light emission device.

[0015] Figs. 7(A) and 7(B) are a section view and a circuit diagram of a semiconductor device to which a bipolar transistor according to the present invention is applied for driving a light emission device.

[0016] Figs. 8(A) and 8(B) are a section view and a circuit diagram of a device to which the FET according to the present invention is applied for controlling a memory device.

[0017] Fig. 9 is a characteristic view of a transistor of the present invention.

Preferable Embodiments of the Invention

(1) Field Effect Transistor (FET)

[0018] A section view of a first embodiment of a transistor according to the present invention is shown in Figs. 1(A) and 1(B). As shown in Fig. 1(A), the transistor of the first embodiment relates to a FET, and comprises a channel layer 11, a source 12, a drain 13, a gate 14, a gate insulating layer 15 and a substrate 16. The channel layer 11 is formed on the substrate 16. On the channel layer 11, formed are the gate insulating layer 15, the source 12 and the drain 13. The gate 14 is formed on the gate insulating layer 15.

[0019] A modification of a first embodiment is shown in Fig. 1(B). In this transistor, the channel layer 11 is formed on the substrate 16. Furthermore, on the channel layer 11, the source 12 and the drain 13 are formed by an ohmic junction, and the gate 14 is formed thereon by a Schottky junction. In this embodiment, since the transistor lacks the gate insulating layer 15 unlike that of Fig.

1(A), a proper gap is provided between the gate 14 and the source 12 and between the gate 14 and the drain 13.

[0020] Materials of the respective constituent components will be described below.

[0021] Firstly, the channel layer 11 is formed of a transparent semiconductor. As the material of the transparent channel layer 11, any of zinc oxide ZnO , zinc magnesium oxide $\text{Mg}_x\text{Zn}_{1-x}\text{O}$, zinc cadmium oxide $\text{Cd}_x\text{Zn}_{1-x}\text{O}$, cadmium oxide CdO or the like can be used. Either a material doped with n and p-type impurities or a material undoped with them may be used.

[0022] Secondly, a transparent electrode is used either for all of the source 12, the drain 13 and the gate 14 or for any of them. As the transparent electrode, a transparent conductive material such as conductive ZnO is used, which is doped with any one of group III elements (B, Al, Ga, In, Tl), group VII elements (F, Cl, Br, I), group I elements (Li, Na, K, Rb, Cs) and group V elements (N, P, As, Sb, Bi) or undoped with them. Herein, when these elements are doped, a doping amount can be set properly. For example, though $\text{n}^{++}\text{-ZnO}$ doped with n-type elements at a high concentration can be used, elements to be doped are not limited to this. Moreover, as the source 12, the drain 13 and the gate 14, transparent conductive materials such as In_2O_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$ can be used in addition to these. Besides these transparent materials, metals such as Al and Cu and electrode materials such as highly doped semiconductor polysilicon which is untransparent may be used. Moreover, it is possible to adopt a transparent material and a non-transparent material together.

[0023] Thirdly, as the gate insulating layer 15, a transparent insulating material such as insulative ZnO doped with an element which can take a valence of 1 as a valence number or doped with group V element is used. As the element which can take the valence of 1, for example, group I elements (Li, Na, K, Rb, Cs), Cu, Ag, Au or the like are enumerated. As the group V element, N, P, As, Sb, Bi or the like are enumerated. As the gate insulating layer 15, in addition to these materials, a transparent insulative oxide material such as Al_2O_3 , MgO , CeO_2 , ScAlMgO_4 and SiO_2 can be used. Furthermore, a transparent insulator such as vinyl and plastic may be used. It should be noted that the gate insulating layer 15 is preferably made of a high insulative material offering a good lattice matching with the material of the channel layer 11. If the channel layer 11 is made of zinc oxide, for example, ScAlMgO_4 or the like are used. These materials are in conformity with each other in their lattice constants in all planes thereof within 1 %, and these materials can be epitaxially grown mutually. Moreover, by using a high dielectric material for the gate insulating layer 15, it is also possible to allow the transistor itself to possess a memory function. As the high dielectric material, for example, $\text{Zn}_{1-x}\text{Li}_x\text{O}$, $\text{Zn}_{1-x}(\text{Li}_y\text{Mg}_{x-y})\text{O}$ or the like can be used.

[0024] Fourthly, as the substrate 16, insulative materials are mainly used. When it is intended that the sub-

strate is made to be transparent, for example, glass, sapphire, plastic or the like can be used as a transparent material. Furthermore, materials that are untransparent may be used as the substrate depending on purposes. For example, for the purposes in which transparency is required as a liquid crystal display screen or the like, a transparent substrate should be used. When a zinc oxide single crystal or a ScAlMgO_4 single crystal as one of materials having the most excellent property is used for the substrate 16, the transparent channel layer 11, or the source 12 and the drain 13 can be grown epitaxially on the substrate. Although some grain boundaries exist on the substrate made of a sapphire single crystal, it is possible to grow the channel layer 11 or the like epitaxially. Moreover, by using the glass substrate, though an in-plane orientation is random, it is possible to control the orientation in a thickness direction as c-axis, and the transistor of this embodiment can show sufficient characteristics as a driving circuit of a display device.

[0025] In Figs. 2(A) and 2(B), section views of second and third embodiments of a transistor according to the present invention are shown. The transistor of the second embodiment shown in Fig. 2(A) relates to a FET, and comprises a channel layer 21, a source 22, a drain 23, a gate 24, a gate insulating layer 25 and a substrate 26. The source 22 and the drain 23 are formed on the substrate 26. The channel layer 21 is formed so as to cover the substrate 26, the source 22 and the drain 23. The gate insulating layer 25 is formed on the channel layer 21. The gate 24 is formed on the gate insulating layer 25. Herein, the gate 24, the gate insulating layer 25 and the channel layer 21 constitute a MIS structure.

[0026] A section view of the third embodiment of the transistor according to the present invention is shown in Fig. 2(B). This transistor is a modification of the second embodiment. In the transistor shown in Fig. 2(B), the gate insulating layer 25 is not formed unlike the transistor shown in Fig. 2(A), and the gate 24 and the channel layer 21 constitutes a Schottky junction structure. When the gate insulating layer 25 is provided like the transistor shown in Fig. 2(A), a limitation to a voltage applied to the gate is small. Contrary to this, when the gate insulating layer 25 is not provided like the transistor shown in Fig. 2(B), withstand voltages between the gate and the source and between the gate and the drain become low. In this case, manufacturing processes are simplified.

[0027] A section view of a fourth embodiment of a transistor according to the present invention is shown in Fig. 3. The transistor of the fourth embodiment relates to a FET, and comprises a channel layer 31, a source 32, a drain 33, a gate 34, a gate insulating layer 35 and a substrate 36. The channel layer 31 is formed on the substrate 36. The gate insulating layer 35 is formed on the channel layer 31, and the gate 34 is formed on the gate insulating layer 35. The source 32 and the drain 33 can be formed by diffusing or ion-implanting impurities thereinto using the gate insulating layer 35 as a mask.

Moreover, as a modification of this embodiment, the gate insulating layer 35 can be omitted by appropriately setting a size of the gate 34 to a certain scale.

[0028] It should be noted that in the foregoing second to fourth embodiments, materials of the constituent components are the same as those described in the first embodiment.

(2) Bipolar Transistor

[0029] A section view of a fifth embodiment of a transistor according to the present invention is shown in Fig. 4. The transistor of the fifth embodiment relates to a bipolar transistor, and comprises a base 41, an emitter 42, a collector 43, a base electrode 44, an emitter electrode 45, a collector electrode 46 and a substrate 47.

[0030] In an npn-type transistor, the emitter 42 and the collector 43 are formed of an n-type transparent semiconductor, and the base 41 is formed by a p-type transparent semiconductor. The base electrode 44, the emitter electrode 45 and the collector electrode 46 are formed respectively on the base 41, the emitter 42 and the collector 43. Similarly, in a pnp-type transistor, the emitter 42 and the collector 43 are formed of a p-type semiconductor as shown in parentheses, and the base 41 is formed of an n-type transparent semiconductor. Since the bipolar transistor can allow a large current to flow therethrough compared to the FET, the bipolar transistor is particularly advantageous when a large current is required for driving a laser or the like.

[0031] The materials of the constituent components will be described below.

[0032] As the n-type transparent semiconductor, for example, n-type ZnO is used. The n-type ZnO is ZnO doped with, for example, group III elements (B, Al, Ga, In, Tl), group VII elements (F, Cl, Br, I). As the p-type transparent semiconductor, for example, p-type ZnO is used. The p-type ZnO is ZnO doped with, for example, group I elements (Li, Na, K, Rb, Cs) and group V elements (N, P, As, Sb, Bi). A doping amount can be set to a proper value depending on a dimension of the device, a thickness thereof, an integration degree thereof and performance thereof.

[0033] Materials of the base electrode 44, the emitter electrode 45, and the collector electrode 46 are the same as those of the source 12, the drain 13 and the gate 14 described in the first embodiment. Specifically, as the transparent electrode, a transparent conductive material such as conductive ZnO doped with any one of group III elements (B, Al, Ga, In, Tl), group VII elements (F, Cl, Br, I), and group I elements (Li, Na, K, Rb, Cs) or conductive ZnO undoped with these materials is used. Herein, when these elements are doped, it is possible to set a doping amount to a proper value. Although n^{++} -ZnO or the like, which are doped with n-type elements with a high concentration, can be used, the doping amount is not limited to this. Moreover, as the base electrode 44, the emitter electrode 45 and the collector elec-

trode 46, a transparent conductive material such as In_2O_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$ can be used in addition to the above described materials. Besides the transparent materials, a metal such as Al and Cu and an untransparent electrode material such as highly doped semiconductor polysilicon may be used. Moreover, transparent or untransparent materials are properly selected and used for all of the electrodes or a part of them.

(3) Stacked Type Semiconductor Device

[0034] A section view of a stacked type semiconductor device is shown in Fig. 5. Fig. 5 shows, as an example, a case where the transistors of the first embodiment are stacked. Specifically, a second transistor is further formed on a transistor which comprises a channel layer 11, a source 12, a drain 13, a gate 14, a gate insulating layer 15 and a substrate 16. At this time, an insulating layer 57 and a conductive shielding layer 58 are formed between the first and second transistors. The conductive shielding layer 58 serves to electrically shield the first and second transistors from one another. As the second transistor, an insulating layer 59 serving as a substrate is formed, and a second source 52 and a second drain 53 are formed thereon. Moreover, a second channel layer 51 is formed so as to cover the insulating layer 59, the second source 52 and the second drain 53, and a second gate insulating layer 55 and a second gate 54 are formed thereon.

[0035] Materials of the insulating layers 57 and 59 may be the same as that of the gate insulating layer 15, and another insulating material identical to that of the transparent substrate 16 may be used. As a material of the conductive shielding layer 58, the same material as that of the source 12, the drain 13 and the gate 14 can be used. By forming the insulating layer 57 or 59 so as to have a thickness larger than that of either the channel layer 11 or the channel layer 51 and the gate insulating layer 15, the conductive shielding layer 58 and the insulating layer 57 or 59 can be omitted.

[0036] When the transistors are stacked upon another, the channel layer 11, the second channel layer 51 or the insulating layer 57 is preferably flattened suitably according to demand. Note that since there is a possibility of increasing cost by adding flattening processes, any of these layers may be flattened properly. Furthermore, as to the number of the stacked transistors, the suitable number of the transistors can be stacked according to demand. Furthermore, the transistors of the foregoing first to fifth embodiments are suitably selected and can be stacked. Still furthermore, the plural kinds of transistors may be selected to be stacked mixedly upon another.

(4) Application to Light Emission Device

[0037] A section view and a circuit diagram of a semiconductor device to which the FET according to the

present invention is applied for driving a light emission device are shown in Figs. 6(A) and 6(B). Reference symbols a, b and c in the section view of Fig. 6(A) correspond to reference symbols a, b and c in the circuit diagram of Fig. 6(B). In this device, a transistor is formed of a channel layer 61, a source 62, a drain 63, a gate 64, a gate insulating layer 65 and a substrate 66. A semiconductor layer 67 is formed on the region of the drain 63, whereby the drain 63 and the semiconductor layer 67 form a light emission portion. Moreover, a source electrode 68, a gate electrode 69 and a light emission portion electrode 60 are provided in this device. As to the light emission portion, when an n-type semiconductor is used for the drain 63, a p-type semiconductor is used for the semiconductor layer 67. On the other hand, when a p-type semiconductor is used for the drain 63, an n-type semiconductor is used for the semiconductor layer 67.

[0038] A transparent semiconductor material identical to that of the gate 64 is used for the semiconductor layer 67, and a transparent electrode material is used for the light emission portion electrode 60. Thus, the light emission portion of this device is enabled to perform a plane light emission in the upward direction in Fig. 6(A). Furthermore, by using a transparent material for the substrate 66, the light emission portion thereof is enabled to perform the plane light emission in the downward direction in Fig. 6(A). In addition, if a light emission zone is equal to an ultraviolet zone, a light emitted from the light emission portion can be converted into a visible light by disposing fluorescent substance either on the light emission portion or under the light emission portion, in other words, on the semiconductor layer 67 and the light emission portion electrode 60 or under the substrate 66.

[0039] A section view and a circuit diagram of a semiconductor device to which the bipolar transistor according to the present invention is applied for driving a light emission device are shown in Figs. 7(A) and 7(B). Reference symbols a, b and c in the section view of Fig. 7(A) correspond to reference symbols a, b and c in the circuit diagram of Fig. 7(B). In this device, a transistor is formed of a base 71, an emitter 72, a collector 73, a base electrode 74, a collector electrode 76 and a base 77. Furthermore, a semiconductor layer 78 is formed on a region of the emitter 72, whereby the emitter 72 and the semiconductor layer 78 form a light emission portion. In addition, a light emission portion electrode 79 is formed on the semiconductor layer 78. When an n-type semiconductor is used as the emitter 72, a p-type semiconductor is used for the semiconductor layer 78. On the other hand, when a p-type semiconductor is used as the emitter 72, an n-type semiconductor is used for the semiconductor layer 78.

[0040] The light emission portion is enabled to perform a plane light emission in the upward direction in Fig. 7(A) by using a transparent semiconductor material identical to that of the base 71 for the semiconductor

layer 78 and a transparent electrode material for the light emission portion electrode 79. Moreover, by using a transparent material for the substrate 77, the light emission portion is enabled to perform a plane light emission in the downward direction in Fig. 7(A). If a light emission zone is equal to an ultraviolet zone, a light emitted from the light emission portion can be converted into a visible light by disposing a fluorescent substrate on the light emission portion or under the light emission portion, in other words, on the semiconductor layer 78 and the light emission portion electrode 79 or under the substrate 77.

[0041] It should be noted that the transistors of the first to third embodiments can be combined with each other for use in driving by forming a light emission portion. Moreover, in the foregoing descriptions, a region continuous with the source or the drain (the collector or the emitter) is used in a part of the light emission portion. In addition to this, a different semiconductor region continuous with the source or the drain (the collector or the emitter) is formed, and this region may be used as a part of the light emission portion. Moreover, the light emission portion may be a light-emitting diode or a laser diode, and a proper light emission device can be formed. Moreover, when the present invention is applied, a semiconductor device, which is entirely transparent, can be fabricated by driving a transparent ZnO light emission device by the use of the transparent transistor. The light emission device can also be made to be partially transparent.

[0042] As the light emission portion, proper structures such as a multilayered reflection film, a double hetero structure and a plane light emission structure are adopted, and they can be combined with each other. Moreover, a plurality of the light emission portions and the transistors are arranged in a matrix fashion, and each of the light emission portions is driven by the transparent transistor, whereby the light emission portion can be applied to a display, an illumination panel, a partial light adjusting panel or the like suitably.

(5) Application to Memory

[0043] A section view and a circuit diagram of a device in which the FET according to the present invention is applied to a control of a memory device are shown in Figs. 8(A) and 8(B). Reference symbols a, b and c of Fig. 8(A) correspond to reference symbols a, b and c of Fig. 8(B). In this device, a transistor is formed of a channel layer 81, a source 82, a drain 83, a gate 84, a gate insulating layer 85 and a substrate 86. On the source 82, formed is a conductive layer 88 made of a transparent conductive material identical to that of the source 82. Furthermore, on a region of the drain 83, formed is a semiconductor layer or a conductive layer 87 with the gate insulating layer 85 interposed therebetween, and thus these constituent components form a capacitor. Herein, though the gate insulating layer 85 is used as an interelectrode insulator of the capacitor, a different

insulating layer from this gate insulating layer 85 may be formed to be used. Furthermore, as an electrode of the capacitor, a region continuous to the source or the drain may be used, or alternatively another semiconductor region or another conductive region, which is connected to the source or the drain, may be used. An electrode material forming the capacitor may be a transparent material or an untransparent material, and the transparent material may be partially used for the electrode material of the capacitor. By properly using the transparent material for these layers and these regions, it is possible to fabricate a memory device which is entirely transparent or partially transparent.

[0044] Also when the bipolar transistor according to the present invention is used, the application to the memory device is possible by forming a capacitor on the substrate properly. Specifically, for example, in the bipolar transistor as in the foregoing embodiments, a capacitor can be formed of a region continuous to the collector or the emitter or a region of another semiconductor or another conductor connected to the collector or the emitter, the insulating layer on this region, and the semiconductor layer or the conductive layer on the insulating layer.

[0045] When the bipolar transistor is applied to the memory device, the memory device can be realized by arranging the transistors and the capacitors in a matrix fashion and by driving the capacitors by the corresponding transistors.

(6) Characteristics

[0046] An example of the characteristic view of the transistor according to the present invention is shown in Fig. 9. Fig. 9 shows an example of a change in a drain current (axis of ordinates) with regard to the FET using ZnO for the channel layer when a drain current (axis of abscissa) is changed in the first embodiment of the present invention. Herein, a thickness of the ZnO channel layer was set to 200 nm, a thickness of the gate insulating layer was set to 100 nm, a gate length was set to 600 μ m, and a gate width was set to 200 μ m. A gate voltage V_G was set to 0 V and a range from -0V to -8V.

(7) Other Applications

[0047] The transistor of the present invention can be fabricated on the same substrate together with the light emission device, the capacitor and other devices. Moreover, the same kind of transistor or different kinds of transistors of the present invention are formed, and transparent materials can be used for wiring between the transistors. The transistors and the devices driven by these transistors can be formed so as to be entirely or partially transparent properly. Moreover, a size, a thickness and a dimension of the transistor can be properly set in accordance with purposes, processes or the like. A doping amount can be properly set in accordance

with manufacturing processes, device performance or the like according to demand.

[0048] Furthermore, as a transparent n-type semiconductor, a transparent n-type semiconductor, a transparent conductive material and a transparent insulating material, the example in which elements are doped on the basis of the ZnO semiconductor was described. However, the present invention is not limited to this. For example, besides zinc oxide ZnO, elements may be doped on the basis of a transparent material such as zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$, cadmium oxide CdO or the like properly.

[0049] Besides the foregoing ways, it is possible to realize a semiconductor device which is entirely or partially transparent by applying to a transistor performing signal processing by driving a detector for detecting light ranging from ultraviolet zone to X-ray zone, to an oxygen sensor, and to a device obtained by combining a sound wave, Surface Acoustic Wave (SAW) or piezoelectric property. Moreover, the present invention enables an electronic circuit to attach on a window glass of a car, a house or the like, a transparent plastic board or the like. The present invention can manufacture computer peripheral equipment for example, a keyboard, a touch panel and a pointing device so as to be transparent. By being transparent, they can be manufactured confidentially, or they can be manufactured so as to be hard to look from some other place. Moreover, it is possible to propose something original in terms of design. In addition to these, an application range of the present invention is very wide.

Industrial Applicability

[0050] The present invention can provide the transistor using the transparent channel layer made of zinc oxide or the like, which is entirely or partially transparent. Specifically, according to the present invention, by using the transparent material such as zinc oxide or the like for the channel layer (conductive layer), the transistor can be provided, which offers no light sensitivity within the visible light region, thus removing a necessity to form the light shielding layer, and increases the area rate of the display portion of the liquid crystal display device or the like.

[0051] Furthermore, according to the present invention, the transparent transistor can be used for various kinds of applications in an optical device field for use in driving a light emission device such as a plane light emission laser and an electroluminescence device and for use in a memory. Still furthermore, according to the present invention, the semiconductor device can be provided, which is used as a transparent electronic device for various kinds of wide applications in addition to a driving circuit requiring no light shielding layer.

Claims

1. A transistor comprising:

5 a transparent channel layer using any one of zinc oxide ZnO, zinc magnesium oxide $Mg_xZn_{1-x}O$, zinc cadmium oxide $Cd_xZn_{1-x}O$ and cadmium oxide CdO; and
10 a source, a drain and a gate, in which a transparent conductive material such as conductive ZnO doped or undoped with any one of group III elements, group VII elements, group I elements and group V elements, a transparent conductor such as In_2O_3 , SnO_2 and $(In-Sn)O_x$, or a untransparent electrode material are used partially or entirely.

2. The transistor according to claim 1, the transistor further comprising:

20 a gate insulating layer using a transparent insulating material such as insulative ZnO doped with elements capable of taking a valence of 1 as a valence number or doped with group V element, a transparent insulating oxide, or a transparent insulator between said transparent channel layer and said gate.

3. The transistor according to claim 1, the transistor further comprising:

30 a gate insulating layer using a high dielectric transparent insulating material such as $Zn_{1-x}Li_xO$ and $Zn_{1-x}(Li_yMg_{x-y})$ between said transparent channel layer and said gate, where said gate insulating layer has a memory function.

4. The transistor according to any one of claims 1 to 3, the transistor further comprising:

40 a transparent insulating substrate on which said transparent channel layer is formed.

5. A semiconductor device, comprising:

45 the transistor according to any one of claims 1 to 4; and
a light emission portion formed of a region continuous to said drain or said source of said transistor or a region of another semiconductor connected to said drain or said source, and a semiconductor layer jointed to said region.

6. A semiconductor device, comprising:

55 the transistor according to any one of claims 1 to 4; and
a capacitor formed by a region continuous to said drain of said source of said transistor or a

region of another semiconductor or a conductor connected said drain and said source, said gate insulating layer or another insulating layer on said region, and a semiconductor layer or a conductive layer on said gate insulating layer or said another insulating layer.

7. A transistor, comprising:

an emitter and a collector, or a base made of a transparent n-type semiconductor such as ZnO doped with group III elements or group VII elements;

a base, or an emitter and a collector made of a transparent p-type semiconductor such as ZnO doped with group I elements or group V elements; and

a base electrode, an emitter electrode and a collector electrode, in which a transparent conductive material such as conductive ZnO doped or undoped with any one of group III elements, group VII elements and group I elements, a transparent conductor such as In_2O_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$, or an untransparent electrode material are used partially or entirely, the base electrode, the emitter electrode and the collector electrode being respectively formed on said base, said emitter and said collector.

8. A semiconductor device, comprising:

the transistor according to claim 7; and
a light emission portion formed of a region continuous to said collector or said emitter of said transistor or a region of another semiconductor connected to said collector or said emitter, and a semiconductor layer jointed to said region.

9. A semiconductor device, comprising:

the transistor according to claim 7, and
a capacitor formed of a region continuous to said collector and said emitter of said transistor or a region of another semiconductor or a conductor connected to said collector or said emitter, an insulating layer on said region, and a semiconductor layer or a conductive layer on said insulating layer.

10. A semiconductor device, wherein the transistor according to any one of claims 1 to 4 and 7 is stacked in plural with an insulating layer therebetween, the insulating layer using a transparent insulating material such as insulative ZnO doped with elements capable of taking a valence of one as a valence number or group V elements, a transparent insulating oxide, or a transparent insulator.

11. A semiconductor device, comprising:

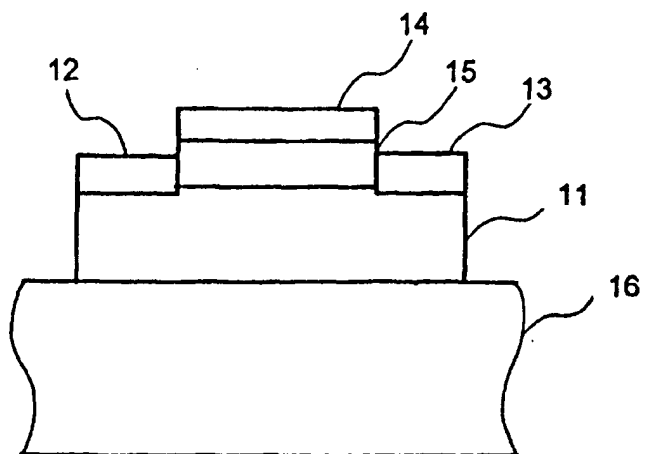
a plurality of the transistors according to any one of claims 1 to 4 and 7,
wherein a transparent conductive material such as conductive ZnO doped or undoped with group III elements, group VII elements, group I elements and group V elements, a transparent conductor such as In_2O_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$, or a untransparent electrode material is used for all of wiring or a part of the wiring between said transistors.

12. A semiconductor device, comprising:

the transistor according to any one of claims 1 to 4 and 7;

an inductor made of a transparent conductive material such as conductive ZnO doped or undoped with group III elements, group VII elements, group I elements and group V elements, or a transparent conductor such as In_2O_3 , SnO_2 and $(\text{In-Sn})\text{O}_x$.

13. A semiconductor device, wherein a plurality of the semiconductor devices according to any one of claims 5, 6, 8 and 9 are arranged in a matrix shape, and a capacitor or a light emission portion is driven by each transistor.



(A)

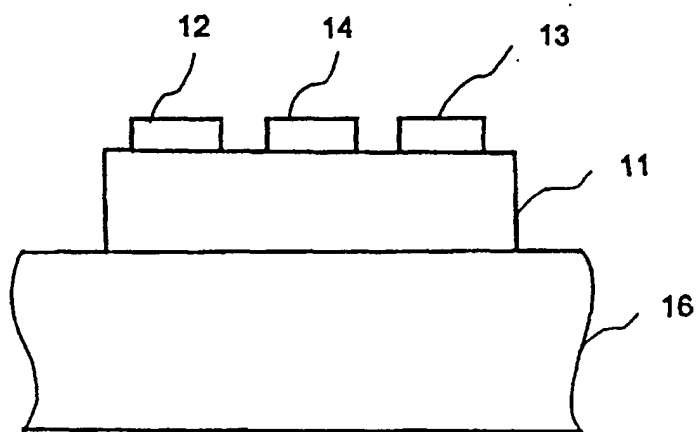
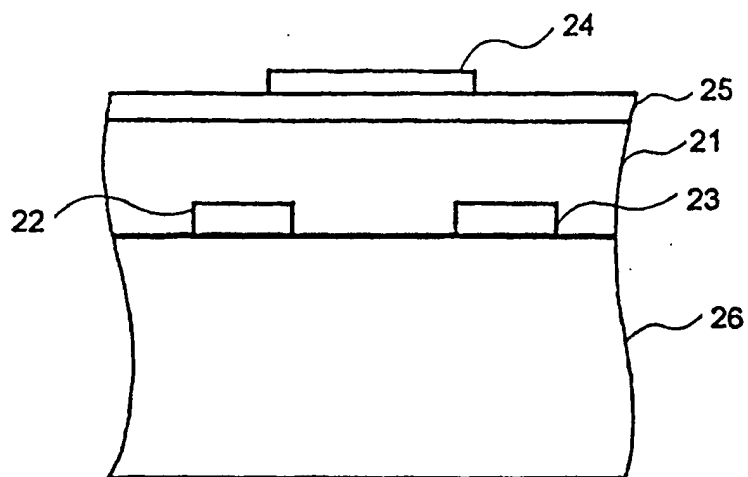
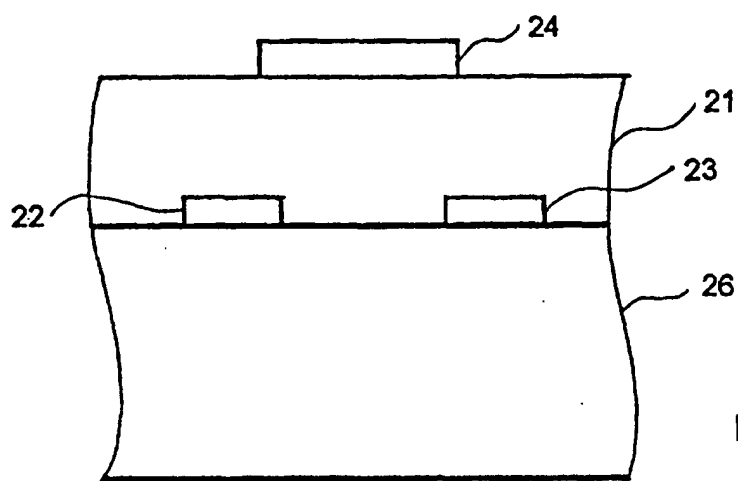


Fig 1

(B)



(A)



(B)

F i g 2

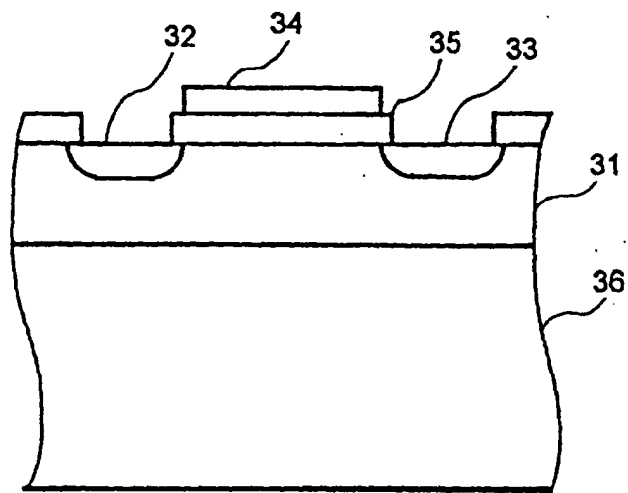


Fig 3

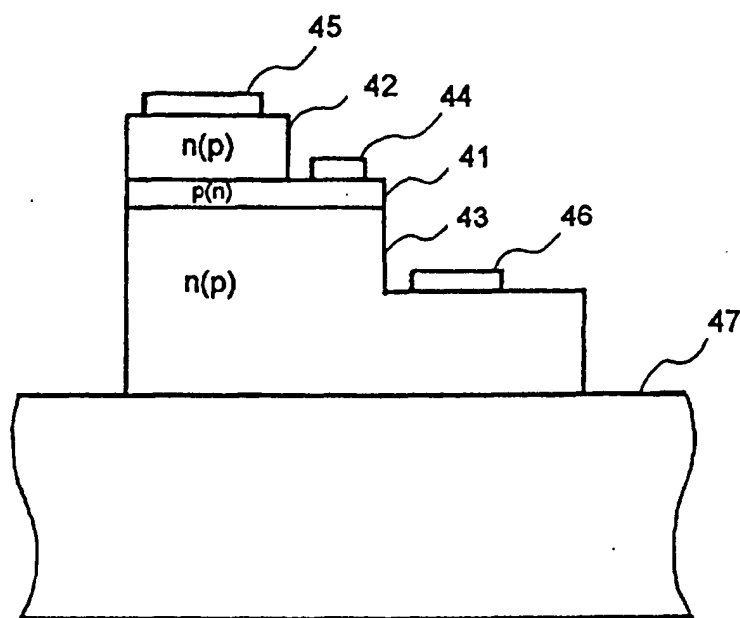


Fig 4

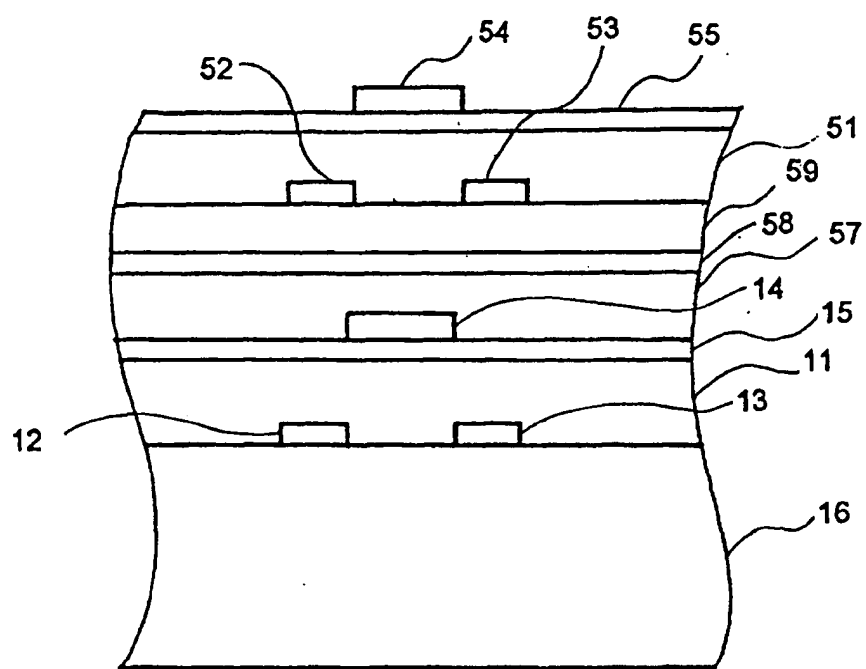


Fig 5

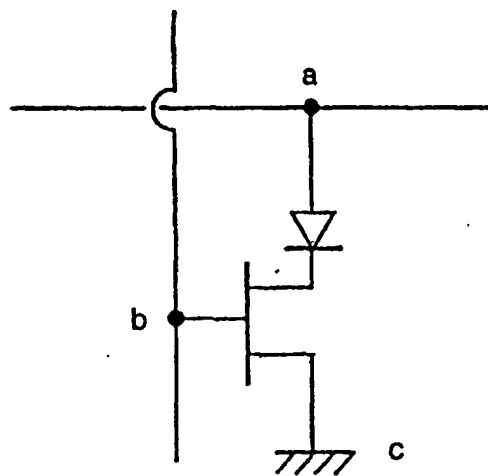
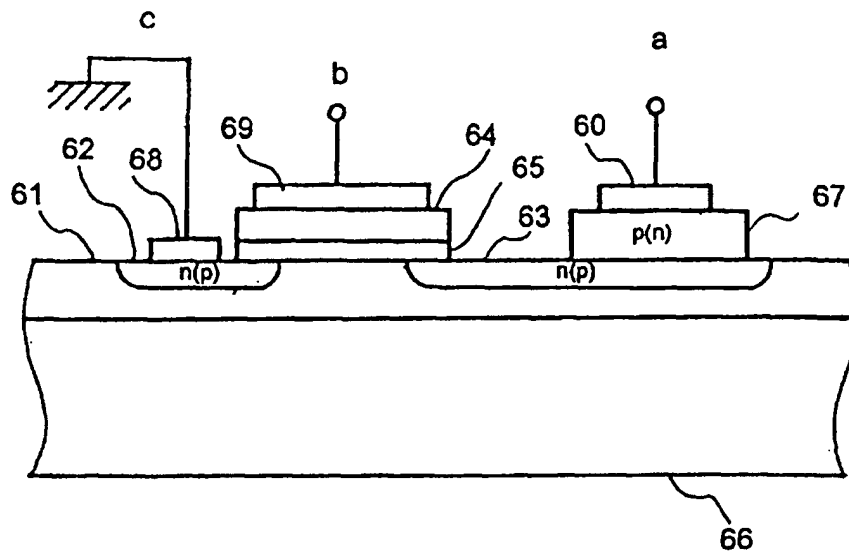
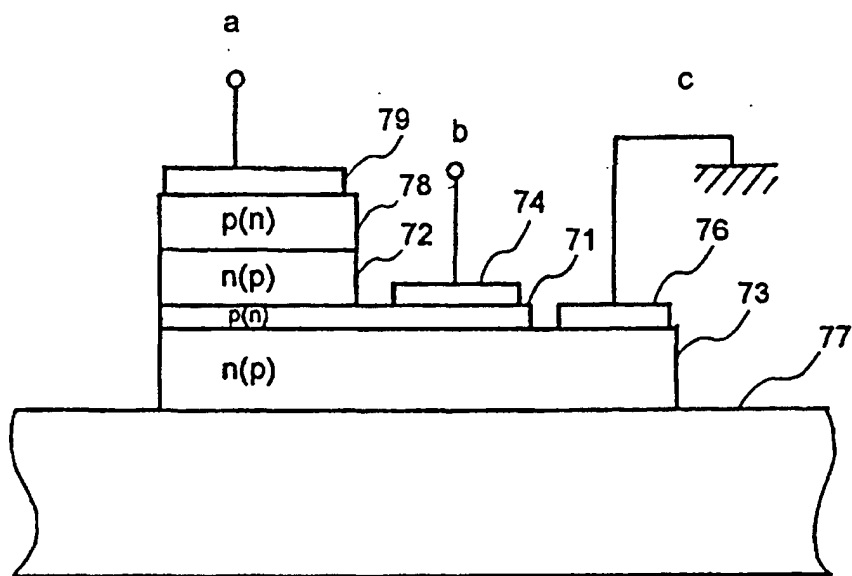
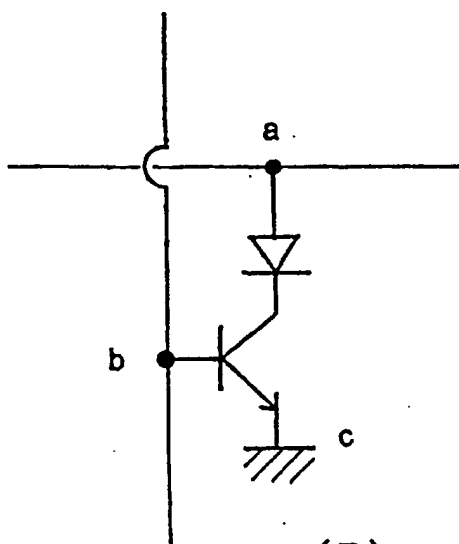


Fig 6

(B)

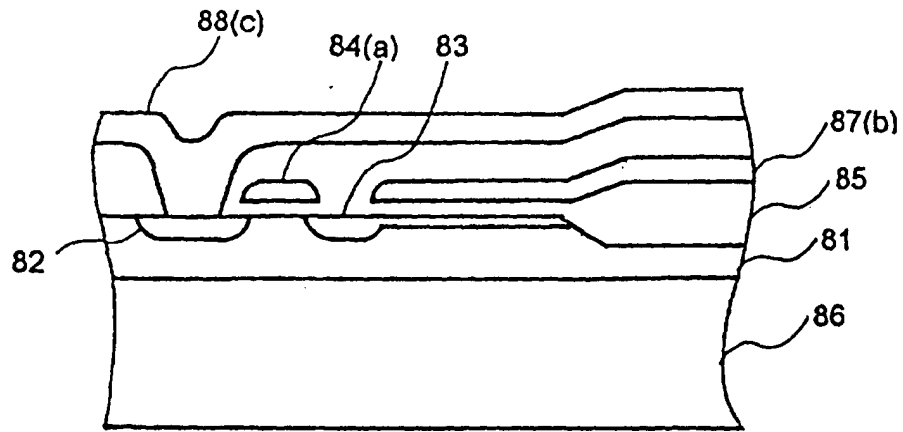


(A)



(B)

Fig 7



(A)

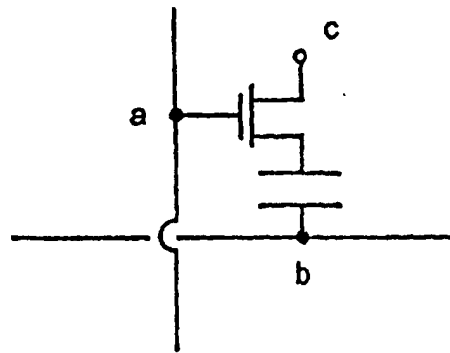


Fig 8

(B)

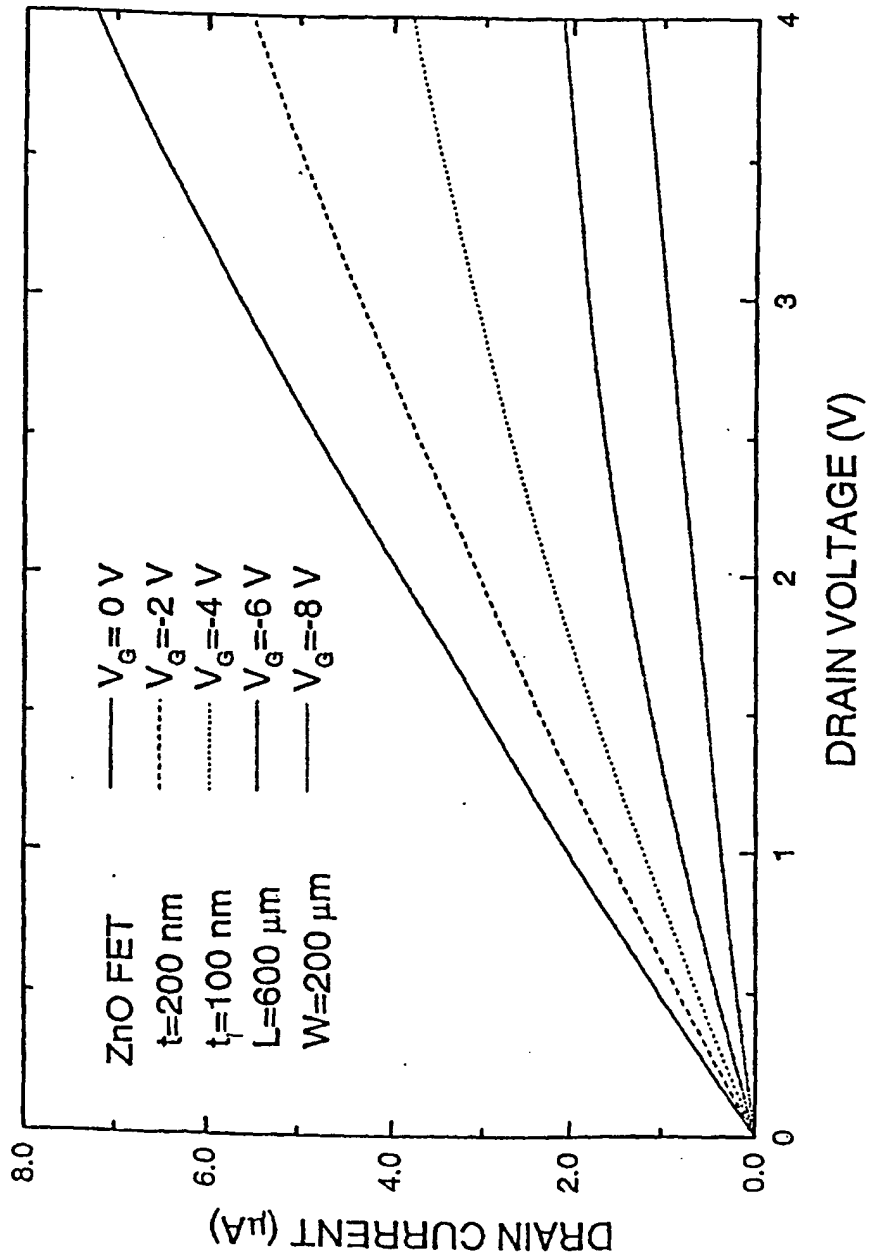


Fig 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP99/06300

A. CLASSIFICATION OF SUBJECT MATTER Int.Cl. ⁷ H01L29/786, H01L29/73, H01L29/80 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Int.Cl. ⁷ H01L29/786, H01L29/73, H01L29/80, H01L33/00 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1972-1999 Kokai Jitsuyo Shinan Koho 1972-1999 Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) INSPEC (DIALOG) JICST (JOIS) CA (STN)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, 5625199, A (Lucent Technologies inc.), 29 April, 1997 (29.04.97), Claim 2 & JP, 9-199732, A Claim 2 & EP, 785578, A	1, 2, 4-6, 10, 11, 13
Y	US, 5744864, A (US. Philips Corporation), 28 April, 1998 (28.04.98), column 4, line 27 to column 6, line 45; Figs. 1 to 4 & JP, 11-1505377, A page 9, line 5 to page 12, line 16; Figs. 1 to 4 & WO, 97006554, A	1-6, 10, 11, 13
Y	JP, 7-114351, A (Casio Computer Co, Ltd.), 02 May, 1995 (02.05.95), Par. No. 6; Fig. 1 (Family: none)	5, 13
Y	US, 4582395, A (Kabushiki Kaisha Suwa Seikosha), 15 April, 1986 (15.04.86), column 5, line 48 to column 6, line 21; Figs. 4 to 5 & JP, 57-132191, A	6, 13
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
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Date of the actual completion of the international search 09 February, 2000 (09.02.00)		Date of mailing of the international search report 22 February, 2000 (22.02.00)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.		Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP99/06300

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	page 4, upper left column, line 12 to upper right column, line 20; Fig. 8. & FR, 2488013, A & GB 2081018, A & DE, 3130407, A & HK, 88887, A	
Y	JP, 63-121886, A (Seiko Epson Corporation), 25 May, 1988 (25.05.88), page 2, upper right column, line 6 to lower left column, line 14; Fig. 1 (Family: none)	6, 13
Y	JP, 56-125868, A (Chiyou LSI Gijutsu Kenkyu Kumiai), 02 October, 1981 (02.10.81), page 1, left column, line 15 to page 2, upper right column, line 1; Fig. 1 (Family: none)	10

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